

Notice of Allowability

Application No.

10/029,394

Examiner

Khiem D. Nguyen

Applicant(s)

KIM ET AL.

Art Unit

2823

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address--

All claims being allowable, PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included herewith (or previously mailed), a Notice of Allowance (PTOL-85) or other appropriate communication will be mailed in due course. **THIS NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RIGHTS.** This application is subject to withdrawal from issue at the initiative of the Office or upon petition by the applicant. See 37 CFR 1.313 and MPEP 1308.

1. ☒ This communication is responsive to 04/21/06.
2. ☒ The allowed claim(s) is/are 7-13.
3. ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
 - a) ☒ All b) ☐ Some* c) ☐ None of the:
 1. ☒ Certified copies of the priority documents have been received.
 2. ☐ Certified copies of the priority documents have been received in Application No. _____.
 3. ☐ Copies of the certified copies of the priority documents have been received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

* Certified copies not received: _____.

Applicant has THREE MONTHS FROM THE "MAILING DATE" of this communication to file a reply complying with the requirements noted below. Failure to timely comply will result in ABANDONMENT of this application.

THIS THREE-MONTH PERIOD IS NOT EXTENDABLE.

4. ☐ A SUBSTITUTE OATH OR DECLARATION must be submitted. Note the attached EXAMINER'S AMENDMENT or NOTICE OF INFORMAL PATENT APPLICATION (PTO-152) which gives reason(s) why the oath or declaration is deficient.
5. ☐ CORRECTED DRAWINGS (as "replacement sheets") must be submitted.
 - (a) ☐ including changes required by the Notice of Draftsperson's Patent Drawing Review (PTO-948) attached
 - 1) ☐ hereto or 2) ☐ to Paper No./Mail Date _____.
 - (b) ☐ including changes required by the attached Examiner's Amendment / Comment or in the Office action of Paper No./Mail Date _____.Identifying indicia such as the application number (see 37 CFR 1.84(c)) should be written on the drawings in the front (not the back) of each sheet. Replacement sheet(s) should be labeled as such in the header according to 37 CFR 1.121(d).
6. ☐ DEPOSIT OF and/or INFORMATION about the deposit of BIOLOGICAL MATERIAL must be submitted. Note the attached Examiner's comment regarding REQUIREMENT FOR THE DEPOSIT OF BIOLOGICAL MATERIAL.

Attachment(s)

1. ☒ Notice of References Cited (PTO-892)
2. ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3. ☐ Information Disclosure Statements (PTO-1449 or PTO/SB/08), Paper No./Mail Date _____
4. ☐ Examiner's Comment Regarding Requirement for Deposit of Biological Material
5. ☐ Notice of Informal Patent Application (PTO-152)
6. ☐ Interview Summary (PTO-413), Paper No./Mail Date _____.
7. ☐ Examiner's Amendment/Comment
8. ☒ Examiner's Statement of Reasons for Allowance
9. ☐ Other _____.

K.N.
July 07th, 2006

DETAILED ACTION

Allowable Subject Matter

1. Claims 7-13 are allowed over prior art of record.

Reasons For Allowance

2. The following is an examiner's statement of reasons for allowance:

After further search and consideration of Applicants' response filed on April 21st, 2006 (see Applicants' arguments in Pages 5 and 6 of the April 21st, response), it is determined that the prior art of record neither anticipates nor renders obvious the claimed subject matter of the instant application as a whole taken alone or in combination, in particular, prior art of record does not teach "sequentially forming an insulating film and a second polysilicon film on the entire structure including said cell region and said peripheral circuit region, the insulating film including an oxide film and a nitride film and being formed under the second polysilicon film; patterning said second polysilicon film and said insulating film so that they can remain only in a give region of said cell region and said peripheral circuit region, respectively, thus forming a control gate of the flash memory cell on the insulating film covering the floating gate in said cell region respectively, and a gate of the code address memory cell on the insulating film covering a surface of the substrate in said peripheral circuit region;"; as recited in the currently amended independent claims 7 and 13.

Claims 8-12 also allowed as being directly or indirectly dependent of the allowed independent base claim 7.

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3. Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

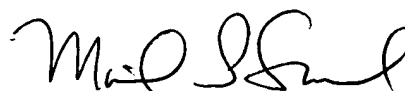
Conclusion

4. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Khiem D. Nguyen whose telephone number is (571) 272-1865. The examiner can normally be reached on Monday-Friday (8:30 AM - 5:30 PM).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Matthew S. Smith can be reached on (571) 272-1907. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

K.N.
July 07, 2006



MATTHEW SMITH
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2800

REPLACEMENT SHEET



OKAY TO ENTER
K.N.
07/07/06

FIG. 1 (PRIOR ART)

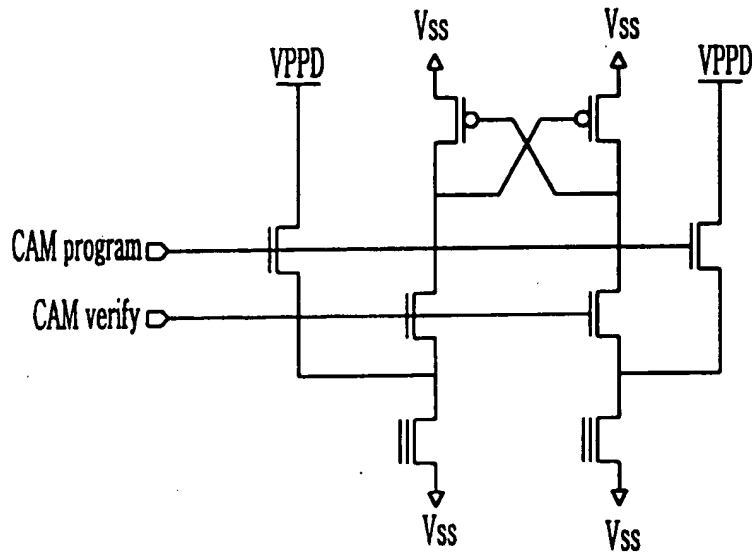
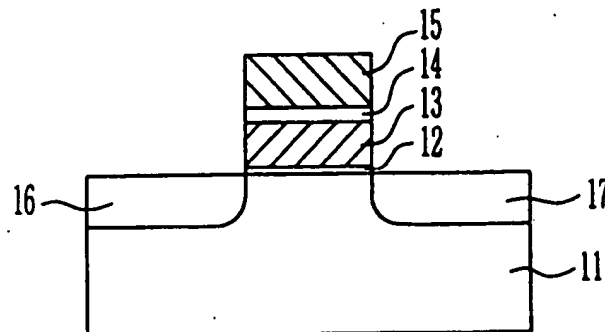


FIG. 2 (PRIOR ART)



013 E JC67
MAR 31 2004
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The diagram illustrates a cross-sectional view of a semiconductor device, divided into two main functional areas: a **Cell** region and a **Peripheral Circuit** region, separated by a vertical line with an 'X' at the bottom.

Cell Region:

- The substrate is labeled **21**.
- A top layer is labeled **25**.
- A stack of three layers is labeled **22**, consisting of **22C** (top, hatched), **22B** (middle, dotted), and **22A** (bottom, hatched).
- A contact **C** is connected to layer **22B**.
- A contact **To** is connected to layer **22A**.

Peripheral Circuit Region:

- The substrate is labeled **21**.
- A top layer is labeled **25**.
- A stack of three layers is labeled **22**, consisting of **22C** (top, hatched), **22B** (middle, dotted), and **22A** (bottom, hatched).
- A contact **23** is connected to layer **22B**.
- A gate **24** is positioned above the stack of layers **22**.